Page 1

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-089212

(43)Date of publication of application : 09.04.1993

(51)Int.Cl. G06F 15/60
G06F 15/20

(21)Application number : 03-247342

(22)Date of filing : 26.09.1991

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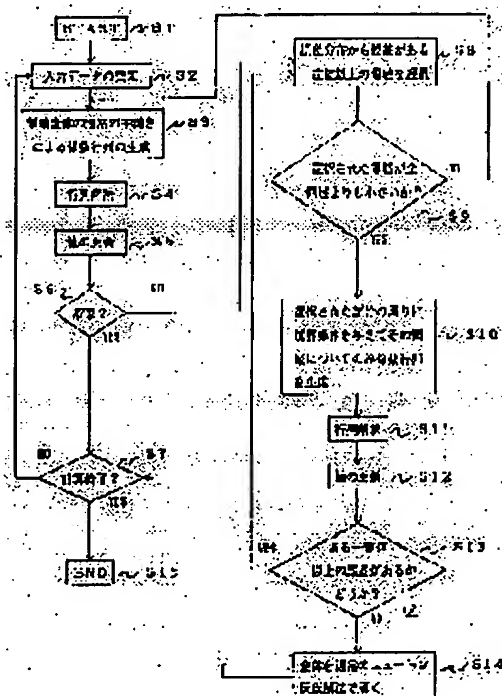
(54) SIMULATING METHOD FOR SEMICONDUCTOR ELEMENT



(57)Abstract:

PURPOSE: To shorten the computing time of simulation of a semiconductor element by numeric value calculation.

CONSTITUTION: Repetitive calculation in the simulation of the semiconductor element is performed by selecting S8 a lattice point area with an error over a constant value from error distribution obtained in convergence decision step S6, updating S9-S12 the value by computing only the area by supplying a boundary condition for a selected area when the selected area is smaller than the whole, repeating procedure to select the next analysis area for the area with the error over the constant value again, and solving the whole by an ordinary repetitive solution S14 at a stage where all the lattice points are housed in a certain range.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

Page 2

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] The simulation approach of the semiconductor device characterized by to have investigated distribution of the amount of corrections after updating a value about all the lattice points in the approach of carrying out simulation of the semiconductor device by numerical calculation, to have chosen the field with the amount of corrections more than a certain constant value, to have given boundary condition only about the field, to have repeated the procedure performed the next count, and to solve the whole after falling within a range with the amount of corrections of all the lattice points.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the simulation approach for numerical calculation to estimate the property of a semiconductor device.
[0002]
[Description of the Prior Art] As the simulation approach of a semiconductor device, a mesh is cut to a semiconductor device field and the method of solving a fundamental equation by numerical calculation is learned.
[0003] Drawing 4 shows the algorithm of such conventional semiconductor device simulation. If this algorithm is explained briefly, simulation will be started at step S25 and count conditions will be inputted at step S26. The amount of corrections is calculated in all the lattice points analyzed at step S27, and the value of each lattice point is updated from the result at step S28. And this procedure is repeated until it judges whether it is converging at step S29, and it returns and converges on step S27, if it is not converging. If it converges, it judges whether the whole count was completed at step S30, and if it is not termination, it will return to step S26 and the above procedure will be repeated.
[0004] With this conventional algorithm, if the lattice point with at least the one big amount of corrections exists, the amount of corrections must be calculated about all the lattice points to whenever [that], therefore computation time will become long.
[0005]
[Problem(s) to be Solved by the Invention] As mentioned above, when numerical calculation was performed in the conventional semiconductor device simulation, the amount of corrections had to be calculated about all the lattice points each time, and there was a problem that computation time became long. This invention aims at offering the simulation approach of a semiconductor device that a solution can be calculated by computation time shorter than before.
[0006]
[Means for Solving the Problem] This invention investigates distribution of the amount of corrections (variation) after updating a value about all the lattice points in the simulation of the semiconductor device by numerical calculation, chooses a field with the amount of corrections more than a certain constant value, gives boundary condition only about the field, repeats the procedure perform the next count, and after it falls within a range with the amount of corrections of all the lattice points, it is characterized by to solve the whole.
[0007]
[Function] When a mesh is cut to a semiconductor device field, numerical calculation is performed about all the lattice points and the amount of corrections is calculated, the amounts of corrections of each lattice point differ for every lattice point, and have the distribution which is in a component field. When the lattice point more than constant value with this amount of corrections is chosen, naturally that field is smaller than all fields. Computation time is shortened compared with the case where repeated calculation will be performed about all the lattice points if it limits to the field, a value is updated and the next count is performed although distribution and the form of the field change with the constant value to set up. In this case, if the constant value which chooses a field is small enough, even if it removes from an analysis field about the lattice point only with the amount of corrections not more than

it, a big calculation error will not be produced.
[0008]
[Example] Hereafter, the example of this invention is explained, referring to a drawing.
[0009] Drawing 1 is the algorithm of semiconductor device simulation using the shade solution method concerning one example of this invention. Step S1 The input data of component structure and others is inputted, and count starts. Step S2 The input data which should be calculated is read and it is step S3. A coefficient matrix is generated about the whole field discretized using a mesh, and it is the coefficient matrix Step S4 It solves using a matrix solution method.
[0010] Step S4 About the calculated amount of corrections, it is step S5. In addition to a trial value, the value of each lattice point is updated, and it is step S6. It judges whether it is converging or not. If it is converging, it is step S7. If it judged whether count would be completed or not and has ended, it will become total-session termination (step S15). If the total session is not completed, it is step S2. It returns, input data is updated and the next count is performed. The above basic method is the same as usual.
[0011] Step S6 When not converging, the field more than the constant value which is with error from the distribution of errors in step S8 is chosen. This constant value is a value which can be set as arbitration according to a service condition. And step S9 It sets and is step S8. The selected field is step S1. If it judges whether it is smaller than the whole defined field and is the same, it is step S2. It returns. This is a case quite far from convergence.
[0012] Step S8 The selected field is step S1. In being smaller than the whole defined field, in step S10, boundary condition is given to the selected field, a coefficient matrix is generated only about the selected field, the determinant is solved at step S11, and it updates a value at step S12. And if it judges whether there is any thing with the value more than the defined constant value (this value can also be set as arbitration according to a service condition) which exists in step S13 among the variation obtained at step S11 and there is a thing more than constant value, it will be step S8. It returns and the same procedure is repeated.
[0013] It is step S1, using as a trial value the value acquired in a series of procedure so far in step S14 when it was judged in step S13 that there is nothing more than constant value. It solves until it converges the whole defined field by the usual Newton iterative solution. Step S7 after converging Procedure of judging whether it being count termination is repeated.
[0014] The magnitude of the matrix which is dispelled at step S11 according to this example is step S4. Compared with the matrix dispelled at step S14, it is small. For example, as shown in drawing 2 , when an error chooses the field more than constant value for the place which should be calculated in all the lattice points 81, as a slash shows, the number of the lattice points of a selection field can be reduced to 25. the constant value which sets up this selection area size and configuration as mentioned above -- it differs. And the part and computation time to which a matrix becomes small become short. moreover, step S3 from -- since these values are close to the convergence solution which should be calculated when the value acquired in a series of procedure to step S13 is used as a trial value -- so much -- step S4 It is repeatedly [usual Newton] few and ends. The whole computation time becomes less than the conventional approach by the above.
[0015] Drawing 3 is the algorithm of the semiconductor device simulation of the example which used the positive solution method. The input data of component structure and others is inputted at step S16, and count starts. The input data calculated at step S17 is read, the amount of corrections is calculated about all the lattice points of an analysis field at step S18, and a value is updated about all the lattice points.
[0016] In step S19, it investigates whether there is any lattice point more than constant value with the amount of corrections calculated at step S18, the following amount of corrections is calculated only about the lattice point which was chosen at step S19 in step S20 in a certain case, and it returns to step S19 again.
[0017] If the lattice point which has the amount of corrections more than constant value at step S19 is lost, it will progress to step S21, the amount of corrections will be calculated about the whole field, and a value will be updated. And it judges whether it is converging at step S22, if it is not converging, the amount of corrections is calculated by returning to step S21 again, and this procedure is repeated until it converges. If it judges whether all count was completed and has not ended at step S23 after converging,

it is step S1. It returns, input data is updated and the same procedure is repeated.
[0018] Also in this example, the whole count of count can be decreased by calculating alternatively only about the lattice point with the amount of corrections more than the constant value which is steps S19 and S20. Moreover, if repeated calculation is performed at steps S21 and S22 by making into a trial value the value calculated in this way, since the value near the solution which should be calculated is given as a trial value, count is completed with small number of occurrence.
[0019]
[Effect of the Invention] When numerical calculation performs simulation of a semiconductor device according to this invention, the field more than constant value with the amount of corrections is chosen and only the field performs repeated calculation, the number of the lattice points to calculate can be reduced and computation time can be shortened [as stated above,].

[Translation done.]

TECHNICAL FIELD

[Industrial Application] This invention relates to the simulation approach for numerical calculation to estimate the property of a semiconductor device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] As the simulation approach of a semiconductor device, a mesh is cut to a semiconductor device field and the method of solving a fundamental equation by numerical calculation is learned.
[0003] Drawing 4 shows the algorithm of such conventional semiconductor device simulation. If this algorithm is explained briefly, simulation will be started at step S25 and count conditions will be inputted at step S26. The amount of corrections is calculated in all the lattice points analyzed at step S27, and the value of each lattice point is updated from the result at step S28. And this procedure is repeated until it judges whether it is converging at step S29, and it returns and converges on step S27, if it is not converging. If it converges, it judges whether the whole count was completed at step S30, and if it is not termination, it will return to step S26 and the above procedure will be repeated.
[0004] With this conventional algorithm, if the lattice point with at least the one big amount of corrections exists, the amount of corrections must be calculated about all the lattice points to whenever [that], therefore computation time will become long.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] When numerical calculation performs simulation of a semiconductor device according to this invention, the field more than constant value with the amount of corrections is chosen and only the field performs repeated calculation, the number of the lattice points to calculate can be reduced and computation time can be shortened [as stated above,].

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As mentioned above, when numerical calculation was performed in the conventional semiconductor device simulation, the amount of corrections had to be calculated about all the lattice points each time, and there was a problem that computation time became long. This invention aims at offering the simulation approach of a semiconductor device that a solution can be calculated by computation time shorter than before.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] This invention investigates distribution of the amount of corrections (variation) after updating a value about all the lattice points in the simulation of the semiconductor device by numerical calculation, chooses a field with the amount of corrections more than a certain constant value, gives boundary condition only about the field, repeats the procedure perform the next count, and after it falls within a range with the amount of corrections of all the lattice points, it is characterized by to solve the whole.

[Translation done.]

OPERATION

[Function] When a mesh is cut to a semiconductor device field, numerical calculation is performed about all the lattice points and the amount of corrections is calculated, the amounts of corrections of each lattice point differ for every lattice point, and have the distribution which is in a component field. When the lattice point more than constant value with this amount of corrections is chosen, naturally that field is smaller than all fields. Computation time is shortened compared with the case where repeated calculation will be performed about all the lattice points if it limits to the field, a value is updated and the next count is performed although distribution and the form of the field change with the constant value to set up. In this case, if the constant value which chooses a field is small enough, even if it removes from an analysis field about the lattice point only with the amount of corrections not more than it, a big calculation error will not be produced.

[Translation done.]

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, the example of this invention is explained, referring to a drawing.
[0009] Drawing 1 is the algorithm of semiconductor device simulation using the shade solution method concerning one example of this invention. Step S1 The input data of component structure and others is inputted, and count starts. Step S2 The input data which should be calculated is read and it is step S3. A coefficient matrix is generated about the whole field discretized using a mesh, and it is the coefficient matrix Step S4 It solves using a matrix solution method.
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[0013] It is step S1, using as a trial value the value acquired in a series of procedure so far in step S14 when it was judged in step S13 that there is nothing more than constant value. It solves until it converges the whole defined field by the usual Newton iterative solution. Step S7 after converging Procedure of judging whether it being count termination is repeated.
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[0015] Drawing 3 is the algorithm of the semiconductor device simulation of the example which used the positive solution method. The input data of component structure and others is inputted at step S16, and count starts. The input data calculated at step S17 is read, the amount of corrections is calculated about all the lattice points of an analysis field at step S18, and a value is updated about all the lattice

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[0018] Also in this example, the whole count of count can be decreased by calculating alternatively only about the lattice point with the amount of corrections more than the constant value which is steps S19 and S20. Moreover, if repeated calculation is performed at steps S21 and S22 by making into a trial value the value calculated in this way, since the value near the solution which should be calculated is given as a trial value, count is completed with small number of occurrence.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The flow chart of semiconductor device simulation using the positive solution method concerning one example of this invention.
[Drawing 2] Drawing showing signs that a rectangle mesh and a part of [the] lattice points are chosen.
[Drawing 3] The flow chart of semiconductor device simulation using the shade solution method concerning other examples of this invention.
[Drawing 4] The flow chart of the conventional semiconductor device simulation.
[Description of Notations]
S1 -S14 -- Processing step.

[Translation done.]

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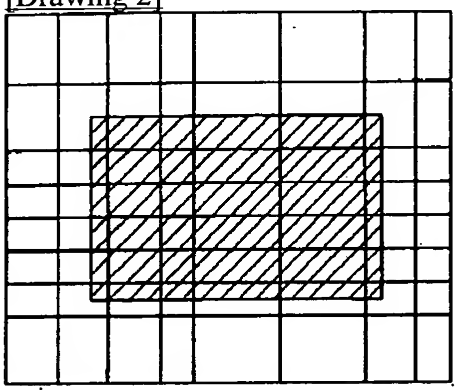
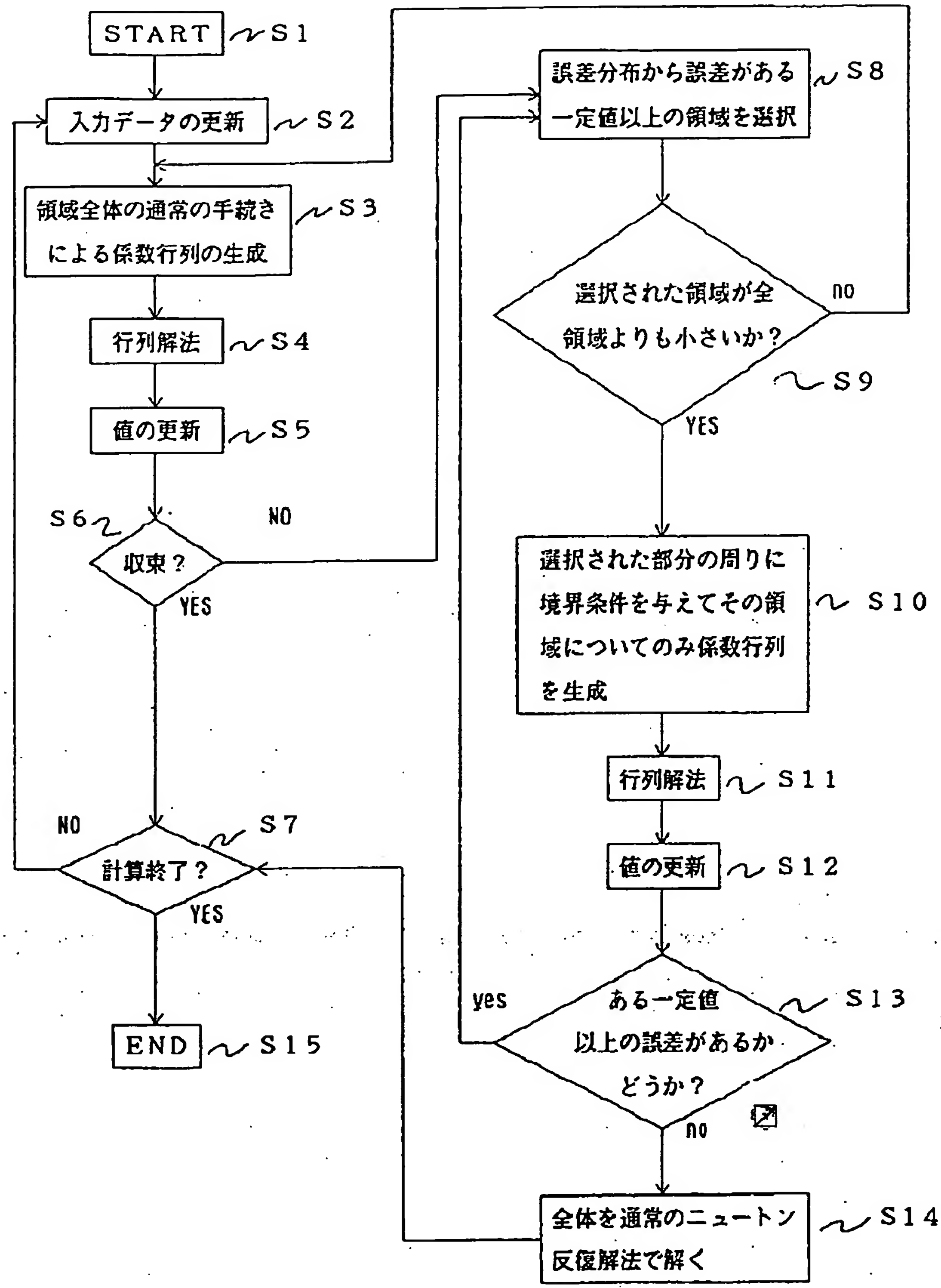
DRAWINGS

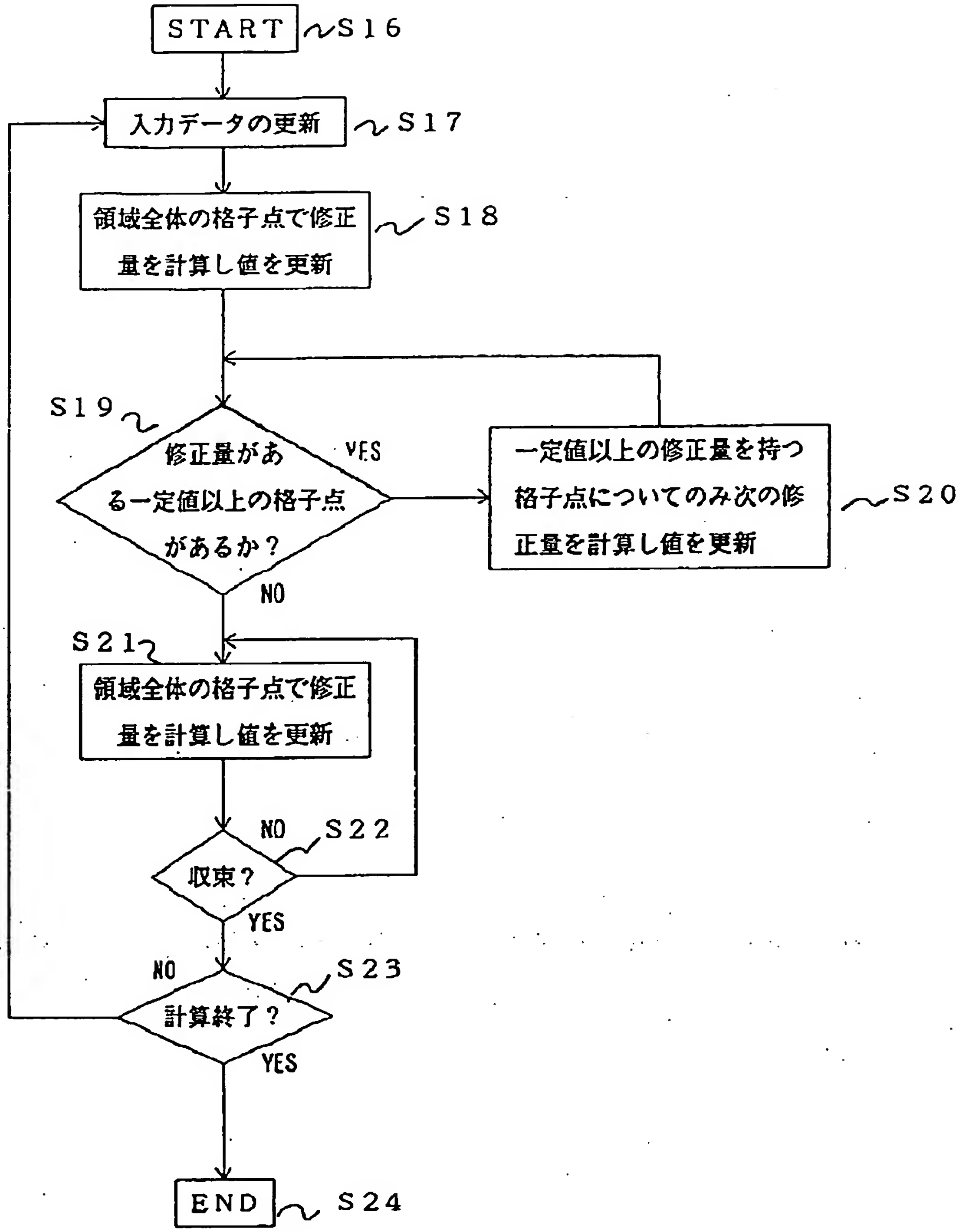
[Drawing 2]



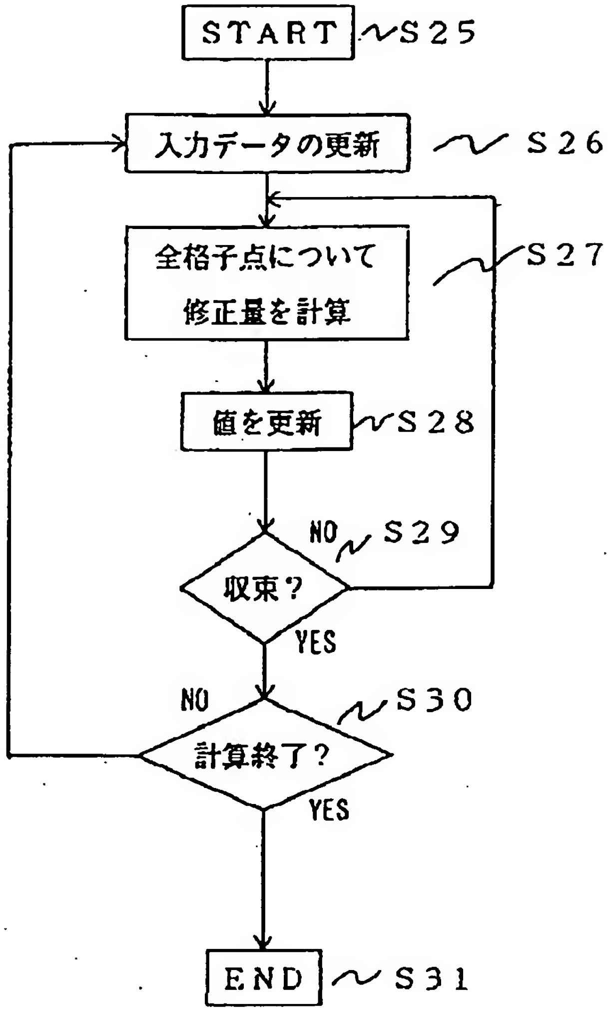
[Drawing 1]


START
S1
入力データの更新
S2
領域全体の通常の手続きによる係数行列の生成
S3
行列解法
S4
値の更新
S5
S6
収束？
NO
YES
誤差分布から誤差がある一定値以上の領域を選択
S8
選択された領域が全領域よりも小さいか？
no
S9
YES
選択された部分の周りに境界条件を与えてその領域についてのみ係数行列を生成
S10
行列解法
S11
値の更新
S12
ある一定値以上の誤差があるかどうか？
S13
yes
no
全体を通常のニュートン反復解法で解く
S14
計算終了？
S7
NO
YES
END
S15

[Drawing 3]


START
S16
入力データの更新
S17
領域全体の格子点で修正量を計算し値を更新
S18
S19
修正量がある一定値以上の格子点があるか？
YES
一定値以上の修正量を持つ格子点についてのみ次の修正量を計算し値を更新
S20
NO
S21
領域全体の格子点で修正量を計算し値を更新
NO
S22
収束？
YES
NO
S23
計算終了？
YES
END
S24

[Drawing 4]



[Translation done.]